

## CLAIMS

1 1. A metallization stack in an integrated MEMS device, the metallization stack comprising:  
2 a titanium-tungsten layer that operatively contacts an electrically conductive  
3 structure in the integrated MEMS device, and  
4 a platinum layer formed over the titanium-tungsten layer.

1 2. The metallization stack of claim 1, wherein the electrically conductive structure is an  
2 active silicon element in a semiconductor substrate of the integrated MEMS device.

1 3. The metallization stack of claim 2 wherein  
2 the titanium tungsten layer contacts the active silicon element via a platinum  
3 silicide layer formed on the semiconductor substrate; and  
4 the semiconductor substrate has an insulating film formed thereon, the insulating  
5 film has a contact hole formed therein, the contact hole exposes a portion of the surface  
6 of the semiconductor substrate at a bottom of the contact hole and the platinum silicide is  
7 formed only on the exposed portion of the surface of the semiconductor substrate.

1 4. The metallization stack of claim 3 wherein the platinum layer is a portion of platinum  
2 wiring formed on the insulating film.

1 5. The metallization stack of claim 1 wherein the integrated MEMS device is an optical  
2 MEMS.

1 6. The metallization stack of claim 1 wherein the integrated MEMS device is a Bio-MEMS  
2 device.

1 7. The metallization stack of claim 6 wherein the platinum layer forms a corrosive resistant  
2 electrode.

1 8. The metallization stack of claim 7 wherein the electrically conductive structure is a  
2 conventional interconnect of the Bio-MEMS device.

1 9. A method of forming a metallization stack for use as a contact structure in an integrated  
2 MEMS device, the method comprising:

3 forming a titanium-tungsten layer that operatively contacts an electrically  
4 conductive structure in the integrated MEMS device, and

5 forming a platinum layer over the titanium-tungsten layer.

1 10. The method of claim 9 further comprising:

2 forming a platinum silicide on a surface of a semiconductor substrate; and

3 wherein the electrically conductive structure is an active silicon element formed  
4 in the semiconductor substrate and the titanium-tungsten contacts the active silicon  
5 element via the platinum silicide.

1 11. The method of claim 10 wherein the forming a platinum silicide step further comprises:

2 depositing an insulating film on the substrate surface;

3                   etching a contact hole in the insulating film;

4                   depositing platinum in the contact hole such that the platinum contacts an  
5 exposed portion of the surface of the semiconductor substrate at a bottom of the contact hole,  
6 and

7                   forming the platinum silicide only on the exposed portion of the surface of the  
8 semiconductor substrate utilizing the deposited platinum.

1       12.   The method of claim 10 wherein the forming a titanium-tungsten layer step further  
2 comprises:

3                   depositing titanium-tungsten on the semiconductor substrate including the  
4 platinum silicide;

5                   depositing a hardmask material over the titanium-tungsten;

6                   removing the hardmask material except for a portion of the hardmask material  
7 above the platinum silicide;

8                   removing the titanium-tungsten except for a portion of the titanium-tungsten  
9 under the hardmask material above the platinum silicide, and

10                  removing the hardmask material above the platinum silicide.

1       13.   The method of claim 12, wherein the hardmask material is AlCu.

1       14.   The method of claim 9, wherein the forming a platinum layer step further comprises:

2                   depositing platinum on the semiconductor substrate including the titanium-  
3 tungsten layer;

4 depositing an oxide hardmask over the platinum;

5 removing the oxide hardmask except for a portion of the oxide hardmask above  
6 the titanium tungsten layer;

7 removing the platinum except for a portion of the platinum under the oxide  
8 hardmask above the titanium-tungsten via a combination of dry etching and wet etching, and

9 removing the portion of the oxide hardmask above the titanium-tungsten layer.

1 15. The method of claim 14, wherein platinum is removed in the removing the platinum step  
2 by sputter etching the platinum in argon followed by wet etching in aqua regia.

1 16. The method of claim 9, wherein the steps further comprise:

2 depositing an insulating film on the substrate surface;

3 etching a contact hole in the insulating film;

4 depositing platinum in the contact hole such that the platinum contacts an  
5 exposed portion of the surface of the semiconductor substrate at a bottom of the contact hole;

6 forming a platinum silicide only on the exposed portion of the surface of the  
7 semiconductor substrate utilizing the deposited platinum;

8 depositing titanium-tungsten on the semiconductor substrate including the  
9 platinum silicide;

10 depositing a hardmask material over the titanium-tungsten;

11 removing the hardmask material except for a portion of the hardmask material  
12 above the platinum silicide;

13 removing the titanium-tungsten except for a portion of the titanium-tungsten  
14 under the hardmask material above the platinum silicide;  
15 removing the hardmask material above the platinum silicide;  
16 depositing platinum on the semiconductor substrate including the titanium-  
17 tungsten layer;  
18 depositing an oxide hardmask over the platinum;  
19 removing the oxide hardmask except for a portion of the oxide hardmask above  
20 the titanium tungsten layer;  
21 removing the platinum except for a portion of the platinum under the oxide  
22 hardmask above the titanium-tungsten via a combination of dry etching and wet etching, and  
23 removing the portion of the oxide hardmask above the titanium-tungsten layer.

1 17. The method of claim 9 wherein the platinum layer and titanium-tungsten layer are  
2 formed by a single plasma etch.

1 18. The method of claim 9 wherein the integrated MEMS device is an optical MEMS.

1 19. The method of claim 9 wherein the integrated MEMS device is a Bio-MEMS device.

1 20. An integrated MEMS device comprising a metallization stack having a contact layer of  
2 platinum and an adhesion layer of TiW.

1 21. The integrated MEMS device of claim 20 wherein the integrated MEMS device is an  
2 optical MEMS device.

1 22. The integrated MEMS device of claim 20 wherein the integrated MEMS device is a Bio-  
2 MEMS device.

1 23. An integrated MEMS device, the device comprising:

2 a semiconductor substrate having an insulating film formed thereon

3 a contact hole formed in the insulating film;

4 a platinum silicide layer formed at the surface of the semiconductor substrate  
5 exposed at a bottom of the contact hole;

6 a titanium-tungsten layer formed on the platinum silicide, and

7 a platinum wire formed on the insulating film, the platinum wiring including a  
8 portion formed on the titanium-tungsten layer.

1 24. The integrated MEMS device of claim 23 wherein the integrated MEMS device is an  
2 optical MEMS.

1 25. The integrated MEMS device of claim 23 wherein the platinum wire is formed by:

2 depositing platinum on the insulating film and the titanium-tungsten layer;

3 depositing an oxide hardmask over the platinum;

4 removing the oxide hardmask except for a portion of the oxide hardmask where  
5 the platinum wire is to be formed;

removing the platinum except for a portion of the platinum under the remaining oxide hardmask via a combination of dry etching and wet etching, and removing the remaining oxide hardmask.

26. The integrated MEMS device of claim 25 wherein the platinum is removed by sputter etching the platinum in argon followed by wet etching in aqua regia.

27. A method of patterning platinum for fabricating a semiconductor device, the method comprising:

depositing platinum on a semiconductor substrate;

patterning the platinum using an oxide hardmask;

etching the platinum using a combination of dry etching and wet etching.

28. The method of claim 27 wherein the combination of dry etching and wet etching comprises sputter etching the platinum in argon followed by wet etching the platinum in aqua regia.

29. The method of claim 27 wherein the patterning step further comprises:

depositing the oxide hardmask on the platinum;

patterning the oxide hardmask using a photoresist;

etching the oxide hardmask according to the pattern such that portions of the oxide hardmask are removed to expose the platinum in areas where the platinum is to be

- 6 removed while leaving portions of the oxide hardmask in areas where patterned platinum is to be  
7 formed, and removing the photoresist.

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